

# **METHOD AND APPARATUS FOR HIGH PERFORMANCE BRANCHING IN PIPELINED MICROSYSTEMS**

## **Abstract of the Disclosure**

A pipelined processor includes a branch acceleration technique which is based on  
5 an improved branch cache. The improved branch cache minimizes or eliminates delays  
caused by branch instructions, especially data-dependent unpredictable branches. In  
pipelined and multiply pipelined machines, branches can potentially cause the pipeline to  
stall because the branch alters the instruction flow, leaving the prefetch buffer and first  
pipeline stages with discarded instructions. This has the effect of reducing system  
10 performance by making the branch instruction appear to require multiple cycles to  
execute. The improved branch cache differs from conventional branch caches. In  
particular, the improved cache is not used for branch prediction, but rather, the improved  
branch cache avoids stalls by providing data that will be inserted into the pipeline stages  
that would otherwise have stalled when a branch is taken. Special architectural features  
15 and control structures are supplied to minimize the amount of information that must be  
cached by recognizing that only selected types of branches should be cached and by  
making use of available cycles that would otherwise be wasted. The improved branch  
cache supplies the missing information to the pipeline in the place of the discarded  
instructions, completely eliminating the pipeline stall. This technique accelerates  
20 performance, especially in real-time code that must evaluate data-dependent conditions  
and branch accordingly.

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